DDR5 SDRAM SODIMM Addendum

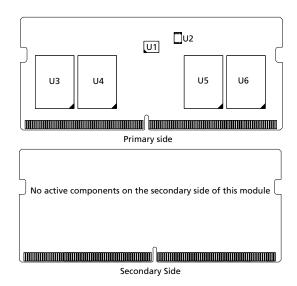## MTC4C10163S1SC – 8GB
16Gb Die Revision A

Features

Information provided here is in addition to or super-sedes information provided in the Micron DDR5 SODIMM Core data sheet.

- DDR5 functionality and operations supported as defined in the component data sheet
- Features and specifications defined in the Micron DDR5 SODIMM core data sheet
- 262-pin, DDR5 small outline dual in-line memory module (DDR5 SODIMM)
- Fast data transfer rate: PC5-4800, PC5-5600
- 8GB (1Gig x 64)
- Single-rank
- 16 internal banks; 4 groups of 4 banks each

Figure 1: 262-Pin DDR5 SODIMM (R/C-C0)

Primary side

No active components on the secondary side of this module

Secondary Side

Options   Marking

- Operating temperature
  – Commercial ($0°C \leq T_{OPER} \leq 95°C$)   C
- Frequency/CAS latency
  – 0.416ns @ CL = 40 (DDR5-4800)   48B
  – 0.357ns @ CL = 46 (DDR5-5600)   56B

Table 1: Addressing

Parameter	8GB
Row address[1]	64K (R0-R15)
Column addres[1]	1K (C0-C9)
Device bank group address[1]	4 (BG0-BG1)
Device bank address per bank group[1]	4 (BA0-BA1)
Device configuration	16Gb (1Gb x 16), 16 banks
Module rank address	1 (CS0_n)

Notes: 1. These parameters represent the logical address state of the CA bus for different commands. Refer to the command truth table in the component data sheet.

Table 2: Part Numbers and Timing Parameters – 8GB Modules

Base device: MT60B1G16,[1] 16Gb DDR5 SDRAM Die Revision A

Part Number	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-$_n$RCD-$_n$RP)
MTC4C10163S1SC48BA1	8GB	1Gb x 64	38.4 GB/s	0.416ns/4800 MT/s	40-39-39
MTC4C10163S1SC56BA1	8GB	1Gb x 64	44.8 GB/s	0.357ns/5600 MT/s	46-45-45

Notes: 1. The data sheet for the base device can be found on micron.com.

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DQ Map

Table 3: Component-to-Module DQ Map

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U3	0	14A	49	U4	0	31A	92
	1	13A	46		1	29A	88
	2	15A	50		2	30A	91
	3	12A	45		3	28A	87
	4	11A	38		4	27A	80
	5	9A	34		5	25A	76
	6	10A	35		6	26A	77
	7	8A	31		7	24A	73
	8	7A	30		8	23A	72
	9	6A	27		9	22A	69
	10	4A	23		10	20A	65
	11	5A	26		11	21A	68
	12	3A	16		12	18A	57
	13	1A	12		13	16A	53
	14	0A	11		14	19A	58
	15	2A	15		15	17A	54
U5	0	5B	194	U6	0	23B	240
	1	4B	191		1	20B	233
	2	6B	195		2	22B	237
	3	7B	198		3	21B	236
	4	2B	183		4	19B	226
	5	0B	179		5	17B	222
	6	1B	180		6	16B	221
	7	3B	184		7	18B	225
	8	14B	217		8	27B	248
	9	12B	213		9	26B	245
	10	15B	218		10	25B	244
	11	13B	214		11	24B	241
	12	11B	206		12	30B	259
	13	8B	199		13	28B	255
	14	10B	203		14	29B	256
	15	9B	202		15	31B	260

I_{DD} Specifications

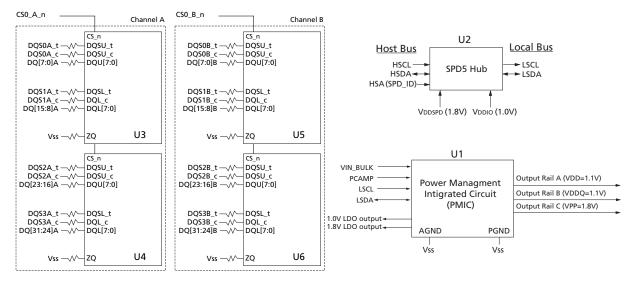## Table 4: DDR5 I_{DD} Specifications and Conditions – 8GB (Die Revision A)

Module I_{DD} is based on PMIC VIN_BULK 5V input current and typical operating temperature. Each I_{DD} parameter includes PMIC efficiency and all DRAM current on all supplies (V_{DD}, V_{DDQ}, and V_{PP}).

Parameter	Symbol	4800	5600	Units
Operating one bank ACTIVATE-PRECHARGE current	I_{DD0}	98	TBD	mA
Operating four bank ACTIVATE-PRECHARGE current	I_{DD0F}	172	TBD	mA
Precharge standby current	I_{DD2N}	74	TBD	mA
Precharge standby non-target command	I_{DD2NT}	166	TBD	mA
Precharge power-down current	I_{DD2P}	65	TBD	mA
Active standby current	I_{DD3N}	81	TBD	mA
Active power-down current	I_{DD3P}	75	TBD	mA
Operating burst read current	I_{DD4R}	537	TBD	mA
Operating burst write current	I_{DD4W}	778	TBD	mA
Operating burst write with write CRC current	I_{DD4WC}	695	TBD	mA
Burst refresh (normal refresh mode) current	I_{DD5B}	248	TBD	mA
Burst refresh (fine granularity refresh mode) current	I_{DD5F}	160	TBD	mA
Burst refresh (same bank refresh mode) current	I_{DD5C}	113	TBD	mA
Self refresh current	I_{DD6N}	31	TBD	mA
Operating bank interleave read current	I_{DD7}	634	TBD	mA
Maximum power saving deep power down mode current	I_{DD8}	23	TBD	mA

Functional Block Diagram

Figure 2: Functional Block Diagram

Notes:
1. The ZQ ball on each DDR5 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.
2. Functional block diagram is for reference only.

Revision History

Rev. C – 10/2021

- Add 5600 speed, IDDs are TBD
- Remove Micron Confidential marking

Rev. B – 08/2021

- Production Release

Rev. A – 01/2021

- Preliminary Release